ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

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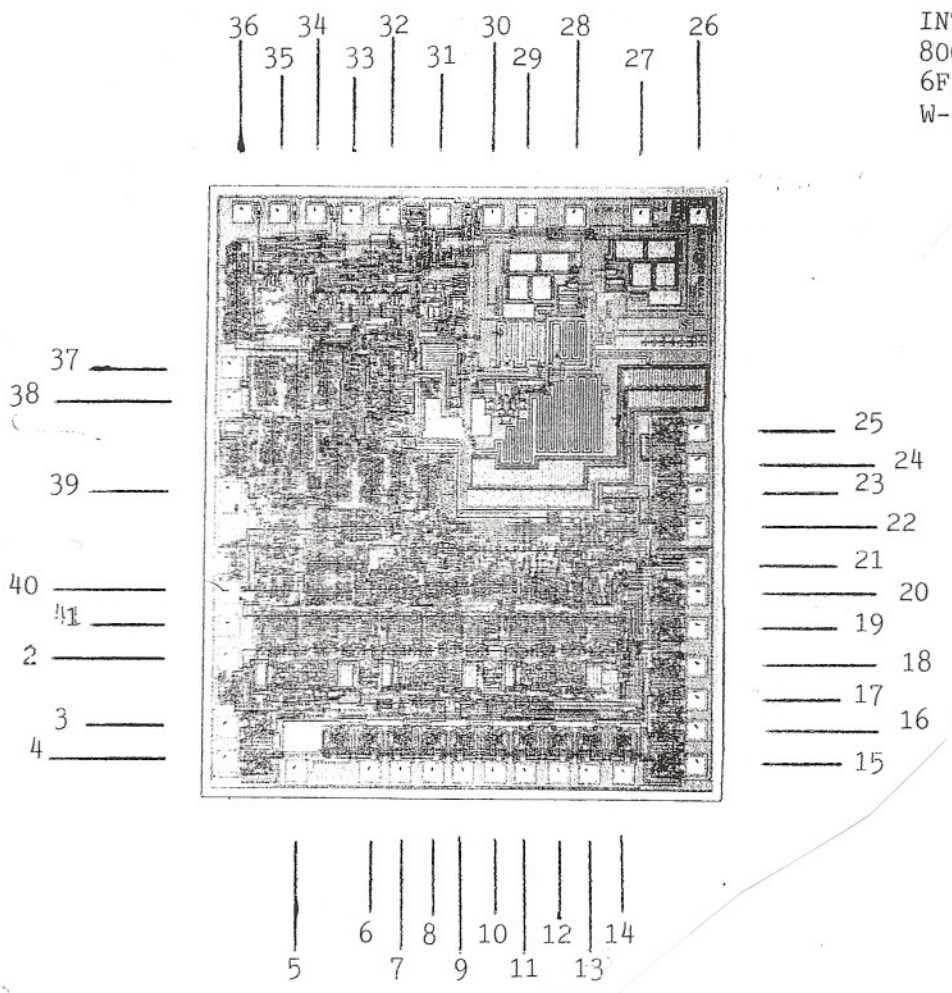
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

STANDARD PACKAGE: 40 PIN D.I.L

Metal Print: ICL7136B
INTERSIL
80CCOPR
6FA
W-OHOLD



PIN/PAD FUNCTION:

1. V+	9. D2	17. F3	25. G2	33. CREF-
2. D1	10. C2	18. E3	26. V-	34. CREF+
3. C1	11. B2	19. AB4	27. INT	35. REFLO
4. B1	12. A2	20. POL	28. BUFF	36. REF HI
5. A1	13. F2	21. BP	29. A/Z	37. TEST
6. F1	14. E2	22. G3	30. IN LO	38. OSC 3
7. G1	15. D3	23. A3	31. IN HI	39. OSC 2
8. E1	16. B3	24. C3	32. COMM	40. OSC 1

APPROVED BY: **DIE SIZE : .149"X .127"** **DATE: 3/28/05**

MFG:Intersil **THICKNESS:** **P/N:ICL7136**